nVIDIA PWM VID Overview

A pulse width modulated I/O that controls the Voltage Regulator VID set point (output voltage) by modulating the duty cycle of the signal sent

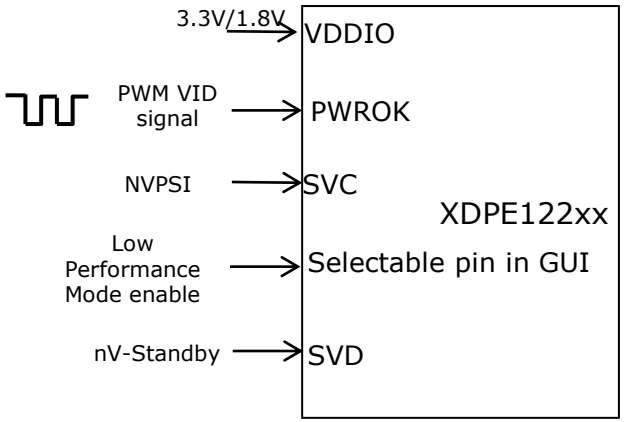
- PWM VID functionality applies to Loop 0 only
- An optional method of control is to digitize an analog voltage (VAUX) and generate an output voltage proportional to this input.

PWM VID implementation allows for

- Wider range of VID set points using a single I/O pin
- VID target change can be communicated in a single cycle
- PSI entry/exit is instantly communicated

nVidia PWM VID connections

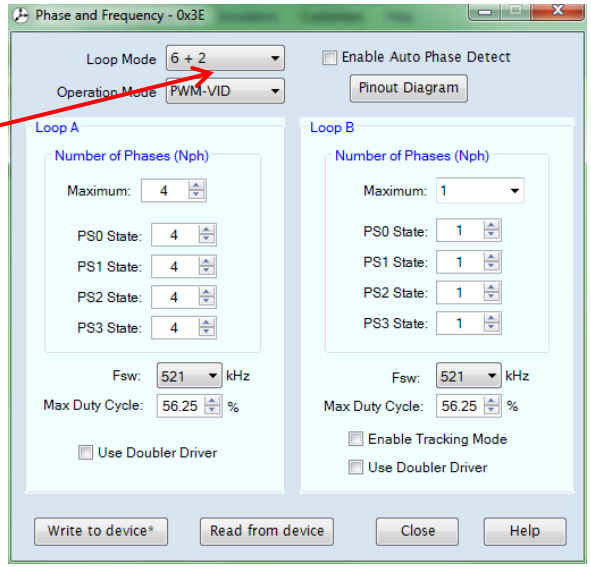
In nVidia PWM mode some pins get a new function in parts that do support the PWM-VID function



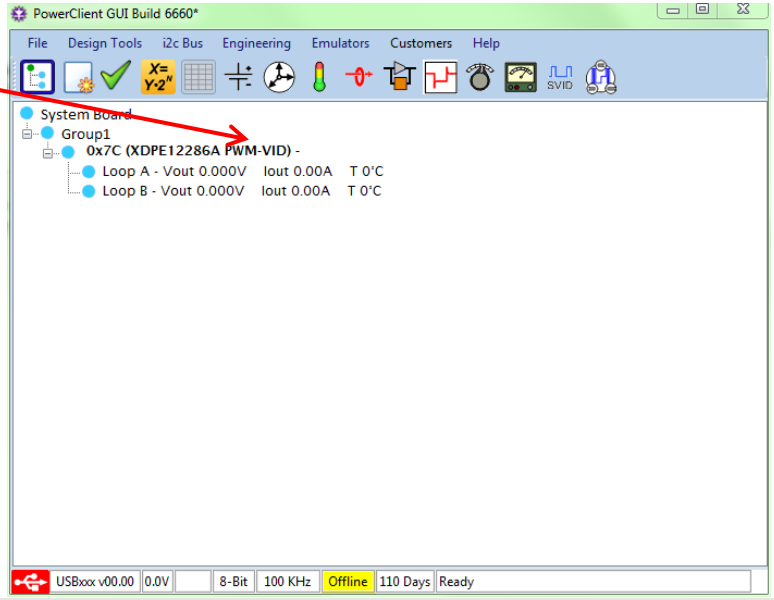
- Check that the right pins are shown
- What are the voltage limits for each signal
- Voltage for VDDIO?

Select nVidia mode

Select the PWM-VID to enter nVidia mode

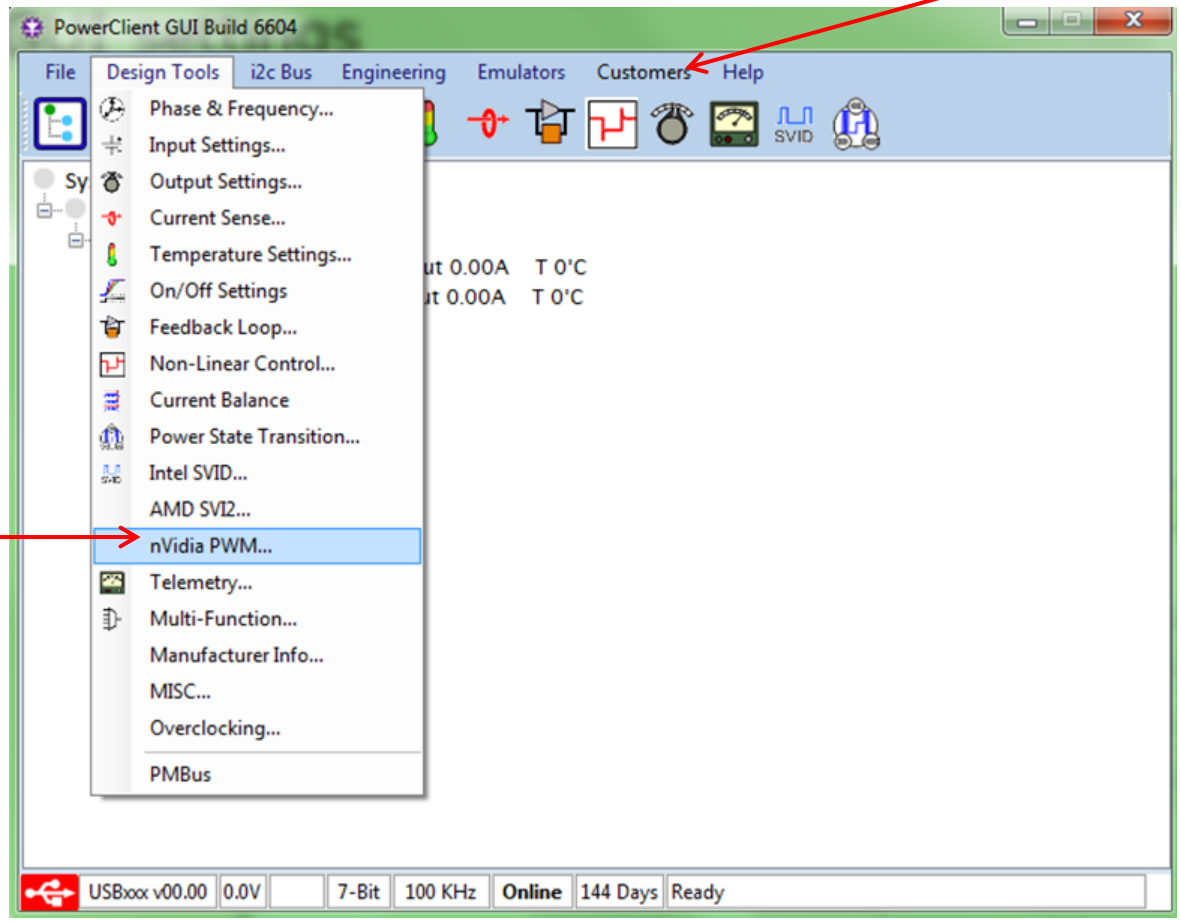


The selected mode is visible after the component name



Find nVidia settings in GUI

You may need a password to activate the nVidia settings. Enter it in the Customers tab
Ask your Infineon FAE if you do not have a password.

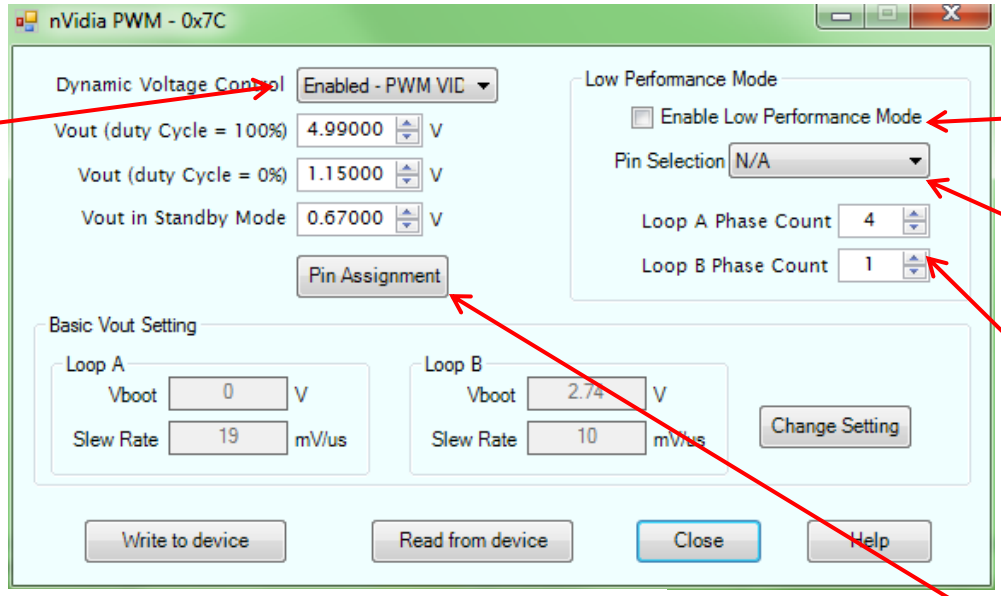


GUI settings

I2C (Disabled) or PWM VID control of Vout (=Enabled)

Start up with Vboot or the value set by the PWM signal.

If PWM signal comes later then starting with Vboot and as soon PWM signal is applied the voltage will change to the voltage set by the PWM



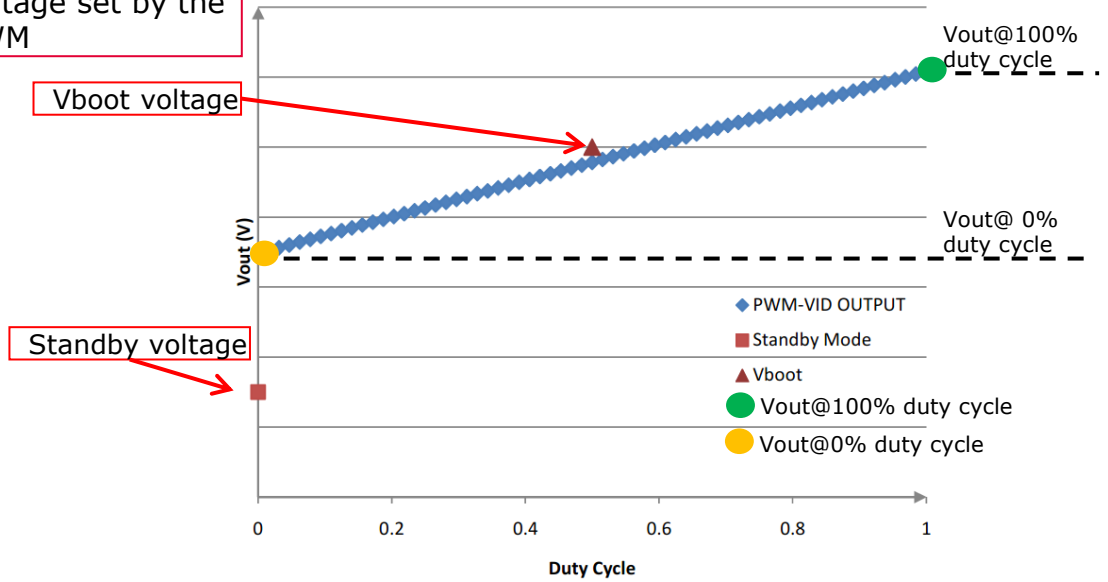
Tick box to enable nVidia Low Performance Mode

Select which pin will act as the enable for Low Performance Mode

Select number of phases when in Low Performance Mode

Pin Assignments

Will show what pins to connect the signals too.



NVidia Digital Solution Requirements

Table 3.1: Register Addresses and Functions

Address (HEX)	Name	Function	Power-On-Reset (HEX)	Access
0x01	PWM-VID	This register configures the settings for PWM-VID dynamic voltage interface..	0X00	R/W
0x02	Offset	8 bit 2's compliment register allows offset of the 00h minimum voltage	0X00	R/W
	Vboot	The voltage when GPU boot up or comes back from standby mode or hibernation.	Flashed	

Table 3.2: PWM-VID Register

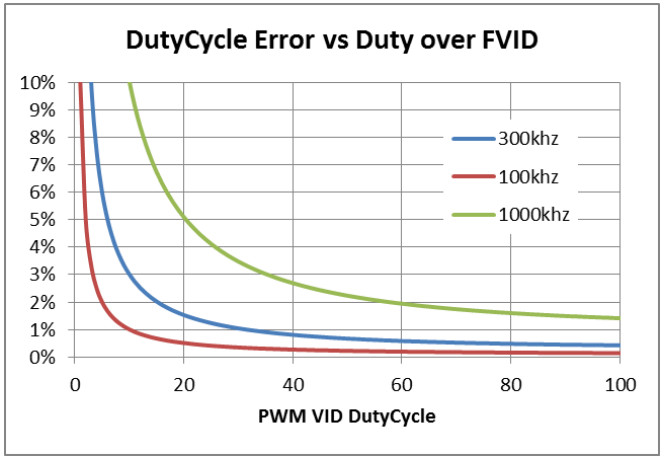
Bit	7	6	5	4	3	2	1	0
Field							Vboot/VID	Mode
Default	0	0	0	0	0	0	0	0

Available registers	Register Address	Description
pwm_vid_mode	01	bit 0 – enables PWM VID mode to control output voltage bit 1 – regulate at the programmed VBoot value when low
pwm_vid_offset	02	non-zero signed value determines the offset vidcodes
pwm_vid_pwr_state	05	sets the internal power state of the controller → 0 is the higest powerstate
pwm_vid_setting	06	when pwm_vid_mode[0]=0, the output voltage is determined by the value of pwm_vid_setting

00:standby
01: Vboot
10: standby
11: PWM VID pin

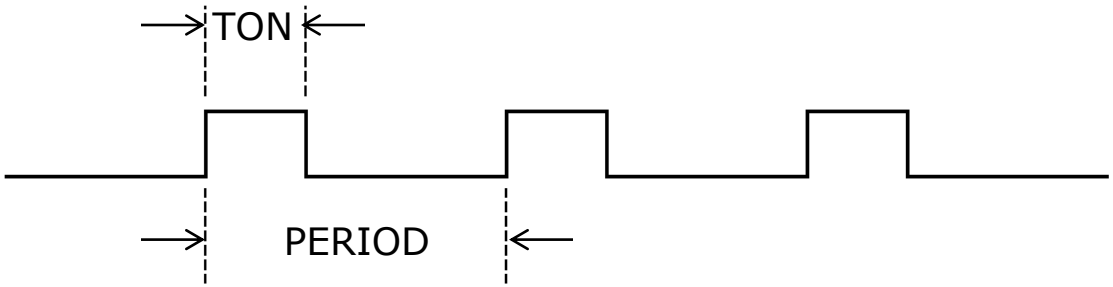
Tahoe Digital Solution

- Page 0x70 dedicated for Digital PWM VID communication
- Digital NVPWM connect directly to the SVD pin
- Signal digitized by 100MHz clock (10ns resolution)
  - Typical FVID 300kHz
  - Usable FVID range 100kHz ←→3MHz
- Digital offset can be added via I2C



Digital PWMVID Measurement

- The dutycycle is calculated as the quotient of the ON time of the NVPWM over the PERIOD of the signal.
  - ON time is measured from the rising edge to the falling edge of the NVPWM
  - PERIOD is measured from a rising edge to the next rising edge



- The calculation is updated on every rising edge of NVPWM
- A continuous moving average of 4 dutycycles calculations is used to set the target voltage

Digital Solution Equations

- Duty = Ton/Period
- Vout = vout_vid_vmin + duty · pwm_vid_slope
  - pwm_vid_slope = (Vmax-Vmin)/(5mV(VIDtable)) per 100% duty cycle change

Other notes

- The SVC pin is used for the NVPSI function. Pulling the pin low would set the VR to a low power state
- TSADC for BTSEN pin
  - Fs=250kHz
  - Q=2.344mV
  - Range 0 ←→ 1.2V

nVidia PWM... Slewrates

- Digital solution
  - the slewrate can be set in the Output Settings window. The fast slew rate setting is used.