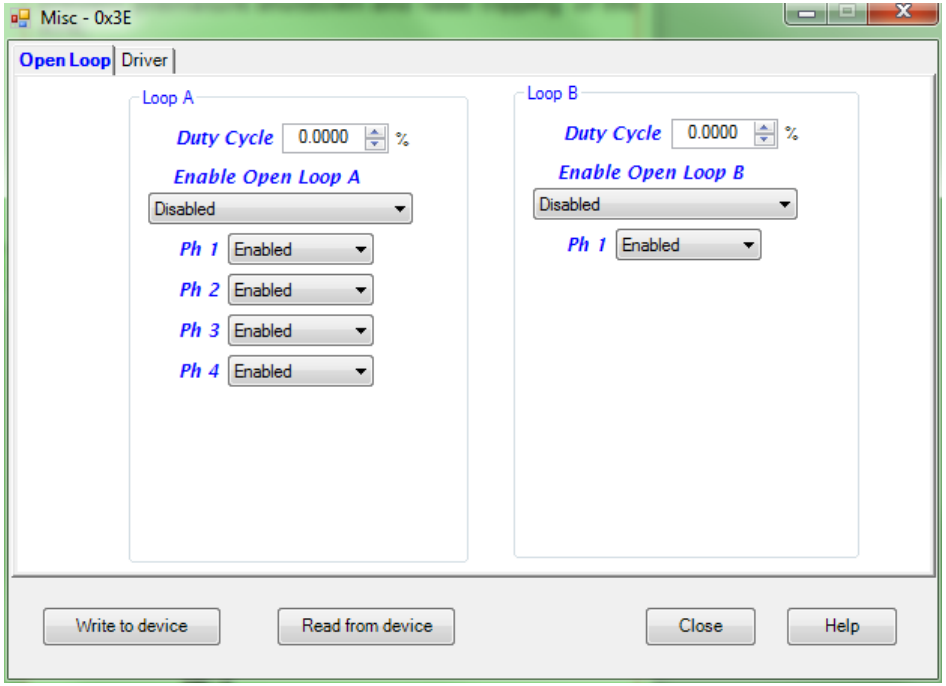
MISC... Open Loop

Duty Cycle
- Fixed duty cycle in open loop

Open Loop Behavior
- *Disabled*: Open loop is disabled
- *Close Loop with Phase Control*
- *Open Loop with Phase Control* controller will send out a fixed **Duty Cycle** .

PH 1/2/3/4/5/6
- *Enabled*: phase 1/2/3/4/5/6 will operate in open loop test
- *Hi-Z*: phase 1/2/3/4/5/6 is not activated.



In open loop mode, output voltage faults (OUVP) protection and all ATR events must be disabled to prevent premature shutdown and false tripping of the ATR.

Step 1: (Important) make sure VR is turned off. i.e. Enable signal low
- It is strongly recommended that the VR be disabled when the user is disabling/enabling open loop function. Otherwise, undesired damage may occur at the power stage.

Step 2: Select the **Open Loop Behavior**
Closed Loop with Phase control
or
Open Loop with Phase Control

Step 3: Set the **Duty Cycle**
- Should be greater than 0%
- To check whether the power stage is operating, a low duty cycle is recommended, typically ~ 10%.

Step 4: Select **PH** x behavior for each Phase
Enabled
or
Hi-Z

Step 5: Click the **Write** button to activate the settings

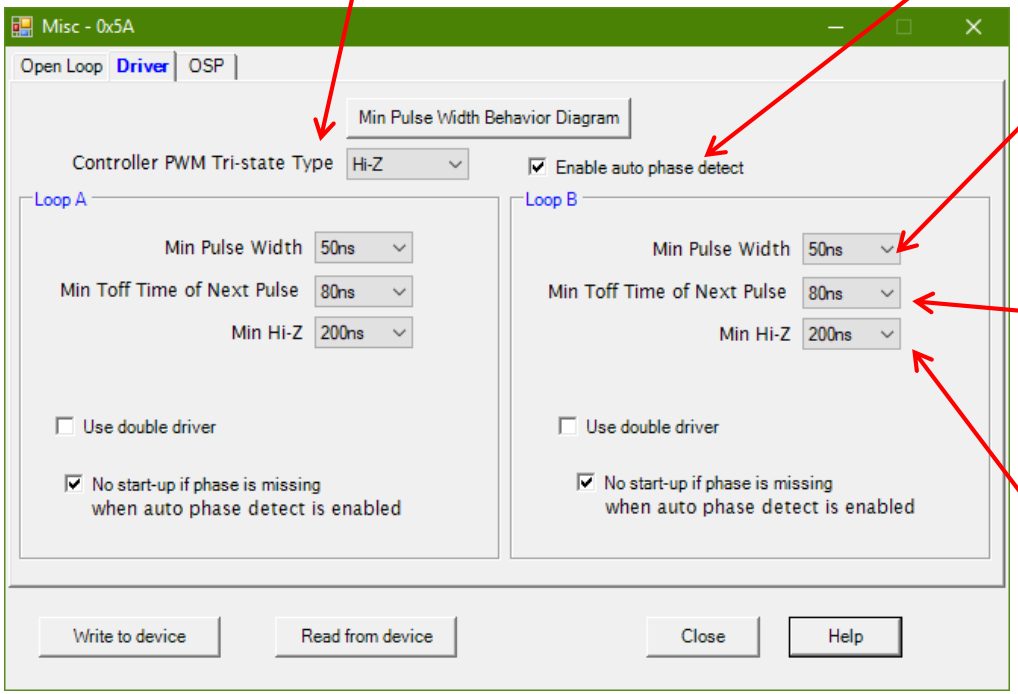
Step 6: turn on regulator i.e. by enable signal

MISC... Driver

Controller PWM Tri-state type

1.5V: PWM will be forced to 1.65V when controller would like to turn off both HSFET and LSFET. This setting is used for drivers which do not have an internal divider to force a Tri-state condition.

Hi-Z: PWM will stay hi impedance when controller would like to turn off both HSFET and LSFET. The voltage on the PWM for Hi-Z will be determined by the driver's internal divider and any stray capacitance may delay the entry to Tri-State.



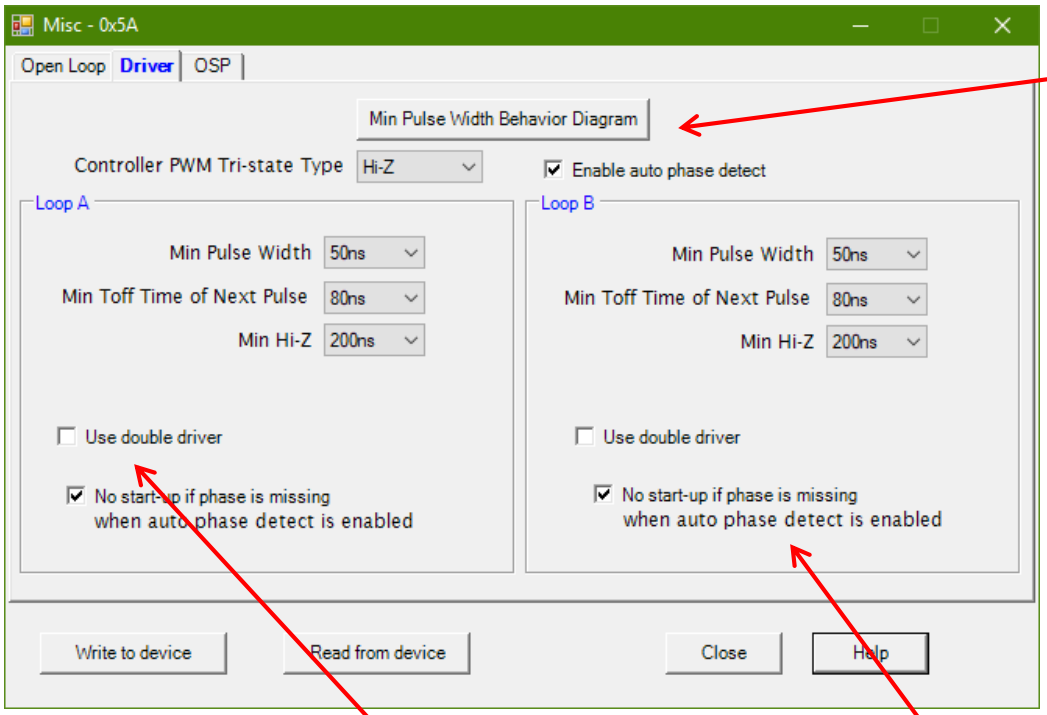
Enable auto phase detect:
During startup the controller can measure each PWM signal and detect if there is a powerstage connected or not.

Min pulse width
Some powerstages do not work well if the PWM is too short. This setting allow to set what the shortest PWM pulse width is to match the need of the powerstage.

Min Toff Time
Minimum time off between PWM pulses

Min Hi-Z
Minimum time for the Hi-Z output.
Allow time for the PWM signal to reach the Hi-Z status as it is not active driven.
Stray capacitance can make it a longer time to enter Hi-Z status and therefor a longer time is needed

MISC... Driver



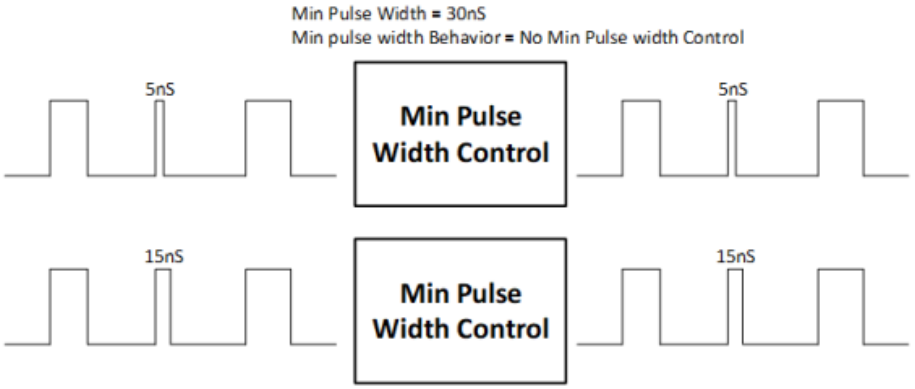
Behavior Diagram
Gives a visual explanation of the different settings and how PWM pulse is treated. See next page in this presentation for diagrams.

Use Double driver
In systems with many phases i.e. 16 a doubler driver can be used that split the PWM signal to two separate Powerstages. But it divide the frequency at same time. Marking this box make controller to know and double switching frequency and know a doubler is used.

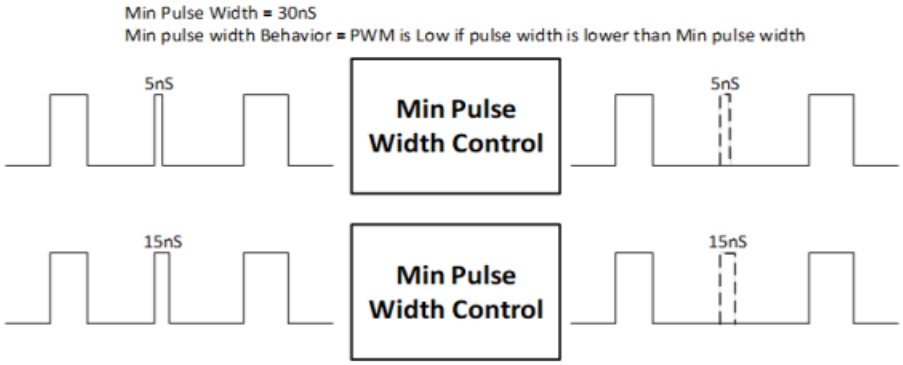
No startup if phase missing:
If the detection of PWM outputs during startup find a not connected powerstage a selection can be mad to start up anyway or not start if all expected powerstages are not detected

MISC... Driver

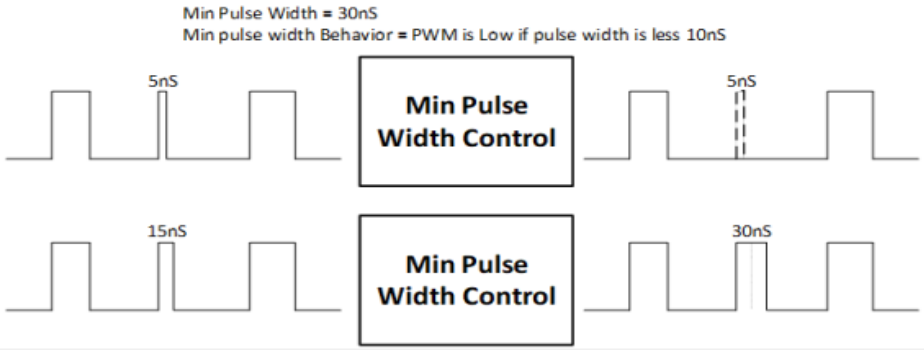
- 1
- No Action



- 2
- Suppressed

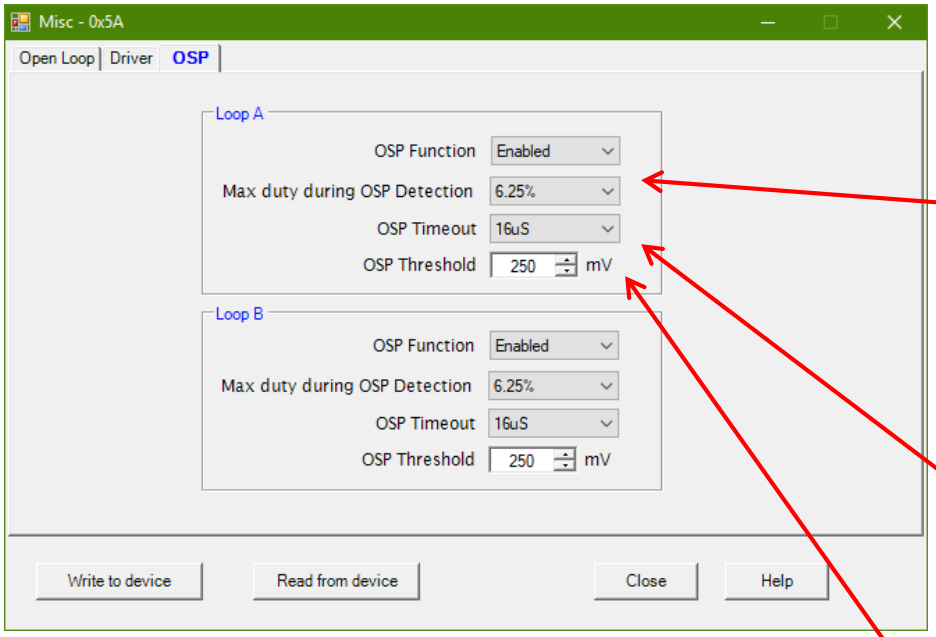


- 3
- Suppress if less than 10us
- Stretch to the set value if longer



MISC... OSP

OSP Output Sense protection
In case of shorted or open feedback this function try to detect this and stop switching if output voltage is not above a threshold within a certain time.



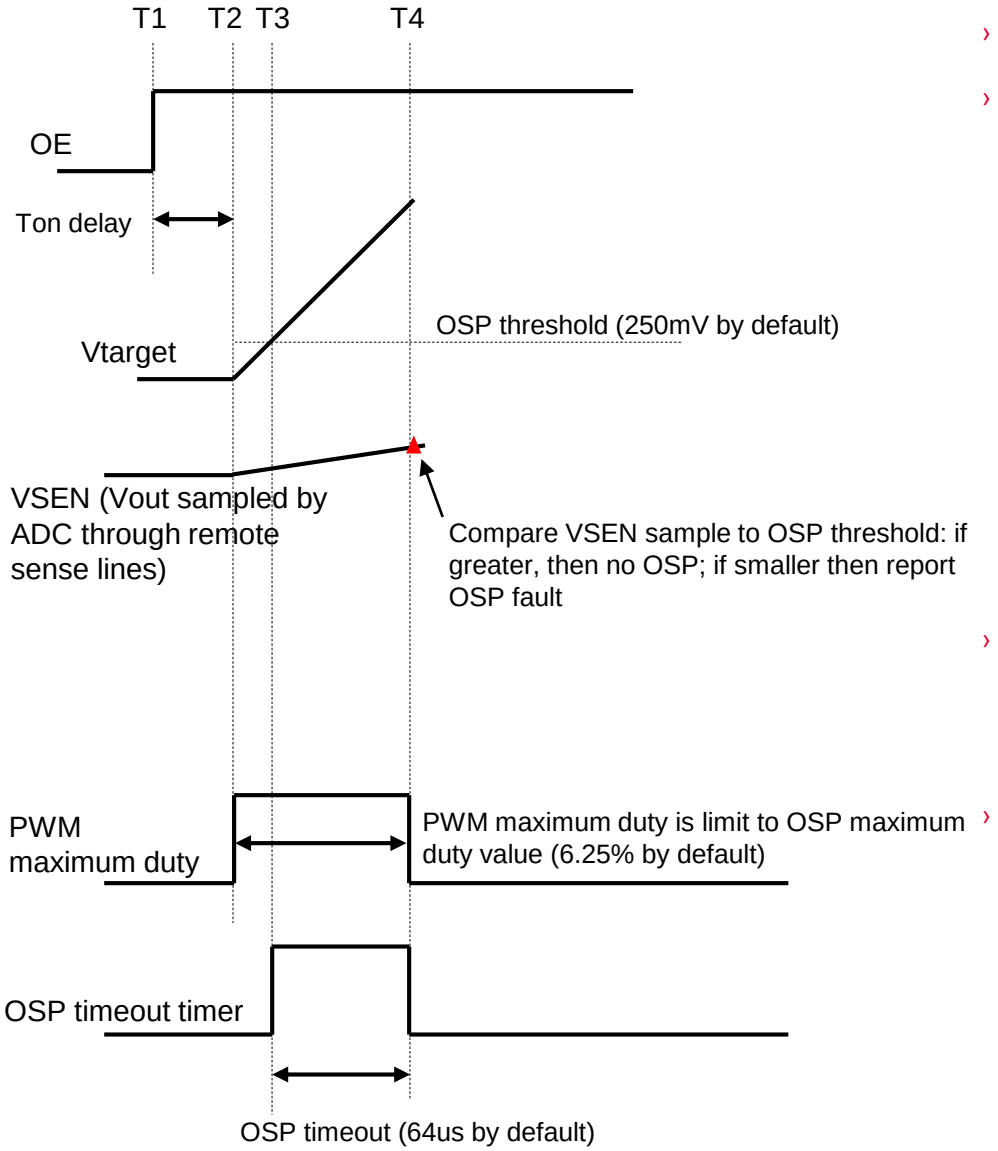
Max Duty during OSP detection
Limits the dutycycle and the output voltage during startup.
Typical 6.25%

i.e. With 12 Volt input and max 6.25% dutycycle Vout can reach 0.75 Volt

OSP timeout
How long time is allowed for Vout to reach the threshold before turning off and signal OPS fault.
Typical 64us When using slow startup slew rates 1mV/us or less the timeout have to be longer 128us. Or even disable OSP function in these cases.

OSP threshold
Voltage expected to be higher than this within the set time to continue normal startup.
Typical 250mV

MISC… OSP timing diagram



- T1: Output enable is asserted.
- T2 (Ton delay after T1)
  - Internal Vtarget starts ramping if Vboot=non zero (note: if Vboot=zero, then no OSP detection until Vtarget starts ramping because of VID change commands.
  - VSEN (Sampled Vout through the differential voltage across remote sense lines):
    - Normally VSEN follows Vtarget.
    - However if remote sense lines are shorted or open, then VSEN voltage can be be near zero.
  - PWM maximum duty is limit to OSP maximum duty cycle from T2 to T4. (this prevent Vout from going too high in case of open feedback)
- T3:
  - Vtarget reaches OSP threshold.
  - OSP timeout timer starts timing.
- T4:
  - OSP timeout timer is expired.
  - Compare VSEN sample to OSP threshold: if greater, then no OSP; if smaller then report OSP fault.
  - PWM maximum duty limit goes back to nominal maximum duty limit.